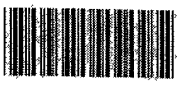
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Dowling, Eric M.
Appl. No.	:	To be Assigned
Filed	:	Herewith
For	:	**EMBEDDED-DRAM-DSP ARCHITECTURE**
Examiner	:	Unknown
Group Art Unit:		Unknown



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PATENT TRADEMARK OFFICE

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Wednesday, February 13, 2002
(Date)

Robert F Gazdzinski, Reg. No 39,990

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to first examination on the merits, please amend the above-referenced application as follows:

IN THE SPECIFICATION:

1. On Page 1, lines 2-4, please delete the paragraph of text beginning with "Reference to Related Applications", and replace it with the following:

--This application is a divisional of U.S. Patent Application Serial No. 10/001,007 filed November 14, 2001, entitled "Embedded-DRAM-DSP Architecture," which claims priority benefit of U.S. Patent Application Serial No. 09/021,933 filed February 11, 1998 of the same title, which claims priority benefit of U.S. provisional application Serial No. 60/054,439 filed August 1, 1997 of the same title. --

2. On page 56, please replace the text on lines 3 through 20 with the following:

--An embedded-DRAM processor architecture includes a DRAM array, a set of register files, set of functional units, and a data assembly unit. The data assembly unit includes a set of row-address registers and is responsive to commands to activate and deactivate DRAM rows and to control the movement of data throughout the system. A pipelined data assembly approach allowing the functional units to perform register-to-register operations, and allowing the data assembly unit to perform all load/store operations using wide data busses. Data masking and switching hardware allows individual data words or groups of words to be transferred between the registers and memory. Other aspects of the invention include a memory and logic structure and an associated method to extract data blocks from memory to accelerate, for example, operations related to image compression and decompression.--

REMARKS

Claims 1-39 are pending in the application. By this paper, Applicant has amended the specification to reflect the divisional status of the application, and to limit the abstract to 150 words or less. By these amendments, no new matter has been added by Applicant. Replacement sheets for these amendments are enclosed herewith.

Claims 1-39 are directed generally to an embedded DRAM apparatus including caching (Group VIII) identified in Par. 1 of the Office Action dated March 1, 2000 in the parent application hereto (U.S. Serial No. 09/021,933 filed February 11, 1998), not previously elected. Note that Claims 1-5 as presented herein are (largely) identical to Claims 19-23 as filed in the parent application.

Applicant specifically reserves the right to prosecute claims of differing or broader scope in a continuation or divisional application.

If the Examiner has any questions or comments which may be resolved over the telephone, he is requested to call the undersigned at (858) 505-1166 or 1167.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: February 13, 2002

By: ______________________

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EMBEDDED-DRAM-DSP ARCHITECTURE

This application is a divisional of U.S. Patent Application Serial No. 10/001,007 filed November 14, 2001, entitled "Embedded –DRAM-DSP Architecture," which claims priority benefit of U.S. Application Serial No. 09/021,933 filed February 11, 1998 of the same title, which claims priority benefit of U.S. provisional application Serial No. 60/054,439 filed August 1, 1997 of the same title.

Background of the Invention

Field of the Invention

This invention relates to the field of microsystems architectures. More particularly, the invention relates to memory access, memory hierarchy and memory control strategies targeted for use in embedded-DRAM (dynamic random access memory) digital signal processors (DSPs) and media processors.

Description of the Related Art

Digital signal processors (DSPs) are microprocessors optimized to execute multiply-accumulate intensive code on arrays of data. Media processors are similar to DSPs, but are further optimized for packed-pixel vector processing and to function in PC and workstation environments. Typical DSP and media processor applications include modems, tone processing for telecommunication applications, cellular communications processing, video compression/decompression, audio processing, computer vision, biomedical signal analysis, and the like. Many of these applications involve the processing of large data arrays that are stored in memory. High-speed on-chip SRAM (static random access memory) is provided on most prior art DSPs in order to allow them to access data rapidly. In many systems, external memory is needed, and such memory has traditionally been implemented with costly SRAM in order keep the DSP from inserting large numbers of wait states while accessing external memory. Larger but slower DRAMs are employed when a very large external memory is needed since fast SRAMs of the same size would be prohibitively expensive in most applications. The use of a slower external DRAM often becomes the bottleneck that limits system performance

EMBEDDED-DRAM DSP ARCHITECTURE

Abstract of the Disclosure

An embedded-DRAM processor architecture includes a DRAM array, a set of register files, set of functional units, and a data assembly unit. The data assembly unit includes a set of row-address registers and is responsive to commands to activate and deactivate DRAM rows and to control the movement of data throughout the system. A pipelined data assembly approach allowing the functional units to perform register-to-register operations, and allowing the data assembly unit to perform all load/store operations using wide data busses. Data masking and switching hardware allows individual data words or groups of words to be transferred between the registers and memory. Other aspects of the invention include a memory and logic structure and an associated method to extract data blocks from memory to accelerate, for example, operations related to image compression and decompression.